AP/LPW
He 5-9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s)	He et al.
Case:	5-9
Serial No.:	10/668,539
Filing Date:	September 23, 2003
Group:	2663
Examiner:	Derrick W. Ferris

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: Barbara Blake Date: November 28, 2005

Title: Connection Admission Control and Routing by Allocating Resources in Network Nodes

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TRANSMITTAL LETTER

Mail Stop Appeal Brief Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

(1) Appeal Brief; and

(2) Copy of Notice of Appeal, filed on September 23, 2005, with copy of stamped return postcard indicating receipt of Notice by PTO on September 26, 2005.

There is an additional fee of $500 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of $500, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully,

Kevin M. Mason

Date: November 28, 2005

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated June 28, 2005, of claims 1 through 23 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Lucent Technologies Inc., as evidenced by an assignment recorded on July 1, 1999 in the United States Patent and Trademark Office at Reel 010077, Frame 0594. The assignee, Lucent Technologies Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 23 are presently pending in the above-identified patent application. Claims 1-4, 6-20, and 22-23 remain rejected under 35 U.S.C. §103(a) as being

unpatentable over Worster (United States Patent Number 6,028,840), and further in view of Mitra (United States Patent Number 5,909,547). The Examiner also indicated that claims 5 and 21 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a method and apparatus regulate the admission control of, and requests for routing of, virtual circuits in a network by determining network resource requirements for the virtual circuits. The method is generalized for the shared-memory architecture of a network node, to allocate a buffer size value, B_i, to an output port, i, for use in the effective bandwidth computation (page 5, line 15, to page 13, line 26). A static allocation policy is utilized to allocate the available buffer, B_{SMF}, to each output port, i. The allocated buffer is determined by selecting a value from a range having a lower bound obtained by partitioning the buffer, B_{SMF}, to evenly divide the buffer space among all the output ports, such that $\sum_i B_i = B_{SMF}$; and having an upper bound obtained by using the total available buffer, B_{SMF}, for each port in their computation of effective bandwidths (page 14, line 1, to page 15, line 26). The network resource requirements are based on a set of parameters used to control the flow of information from a communications device onto the virtual circuit. The requirements for network resources typically include buffer space requirements in network nodes and bandwidth requirements in network links, and the parameter used to control the flow of information are those associated with an access regulator, such as a leaky bucket regulator (LBR). The network resource determination is made for the case where lossless performance in the network is required and in the case where statistical multiplexing with limited loss is allowed (page 5, line 15, to page 13, line 26).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 6-20, and 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Worster, and further in view of Mitra.

ARGUMENT

Independent Claims 1, 11, 22 and 23

Claims 1, 11, 22, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Worster, and further in view of Mitra. In particular, the Examiner asserts that Worster discloses a method and apparatus for connection admission control, but acknowledges that Worster is generally silent on both the location and the type of the buffer memory used and is deficient to the claim in the limitation of "allocating a portion, B_i, of said buffer to each of said output ports." The Examiner asserts that such a claim limitation of allocating a portion of the buffer to each of the output ports would have been obvious to a skilled artisan prior to Applicants' invention. The Examiner further asserts that it would have been obvious to a skilled artisan prior to Applicants' invention to also base the "same equation" on an individual buffer for a shared buffer space as is known in the art based on the *combined teachings of Worster in view of Mitra* (emphasis added).

Appellants note that, as the Examiner acknowledges, Worster does not suggest or disclose "provisioning a portion, B_i, of said buffer to each of said output ports." Thus, Worster does ***not*** *disclose or suggest a buffer portion* B_i and can therefore not disclose or suggest determining buffer space requirements from a set of parameters, wherein a ratio of said effective buffer space requirement b_0 to *said allocated buffer size* B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C, as required by each of the independent claims.

Appellants also note that, although Mitra does "determine (a) provisional allotment of buffer memory space for output ports" in step 415, Mitra does not disclose or suggest determining buffer space requirements from a set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C, as required by

each of the independent claims.

Independent claims 1, 11, 22, and 23 require determining "buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C."

Thus, Worster and Mitra (alone or in combination) do not disclose or suggest determining "buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C," as required by independent claims 1, 11, 22, and 23.

Regarding the Examiner's comments on Elwalid, Appellants note that the cited claims were not rejected in view of Elwalid and that, in the Office Action dated October 6, 2004, the Examiner acknowledges that Elwalid is silent or deficient to the concept of partitioning a common queue into subqueues where each subqueue is dedicated to a specific out port. Appellant also notes that Elwalid does not disclose or suggest an effective bandwidth requirement for multiple output ports sharing the same buffer.

Thus, Worster, Mitra, and Elwalid et al. (alone or in combination) do not disclose or suggest determining "buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C," as required by independent claims 1, 11, 22, and 23.

Claims 3 and 19

Claims 3 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Worster, and further in view of Mitra. Regarding claims 3 and 19, the Examiner asserts that Worster discloses using set parameters such as a lossless effective (bandwidth) (col. 7, lines 20-25).

Claims 3 and 19 require wherein a lossy effective bandwidth, e_l, is obtained from the expression C/K_{max}, where K_{max} is the maximum value of K that satisfies the inequality:

$$P_r\left[\sum_i^K U_i(t) \geq C\right] \leq CLR.$$

Appellants could find no disclosure or suggestion by Worster or Mitra of satisfying the inequality $P_r\left[\sum_i^K U_i(t) \geq C\right] \leq CLR.$

Thus, Worster, Mitra, and Elwalid et al. (alone or in combination) do not disclose or suggest wherein a lossy effective bandwidth, e_l, is obtained from the expression C/K_{max}, where K_{max} is the maximum value of K that satisfies the inequality:

$$P_r\left[\sum_i^K U_i(t) \geq C\right] \leq CLR.,$$

as required by claims 3 and 19.

Claims 4 and 20

Claims 4 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Worster, and further in view of Mitra. Regarding claims 4 and 20, the Examiner asserts that Mitra discloses a shared bandwidth approach (col. 9, lines 25-30; col. 10, lines 1-24).

Claims 4 and 20 require wherein said portion, B_i, of said buffer is allocated to each of said output ports, i, by selecting a value from a range bounded by a lower limit that divides the buffer space, B, among all the ports such that $\sum_i B_i = B_{SMF}$ and an upper limit that allocates said portion, B_i, of said buffer to each of said output ports, i, using a sharing approach where each port uses B in their computation of effective bandwidths. Appellants, however, could find no disclosure or suggestion by Worster or Mitra of allocating a portion, B_i, of a buffer to each of the output ports, i, by selecting a value from a range bounded by a lower limit that divides the buffer space, B, among all the ports such that $\sum_i B_i = B_{SMF}$ and an upper limit that allocates the portion, B_i, of the buffer to each of the output ports, i, using a sharing approach where each port uses B in their computation of effective bandwidths.

Thus, Worster, Mitra, and Elwalid et al. (alone or in combination) do not disclose or suggest wherein said portion, B_i, of said buffer is allocated to each of said output ports, i, by selecting a value from a range bounded by a lower limit that divides the buffer space, B, among all the ports such that $\sum_i B_i = B_{SMF}$ and an upper limit that allocates said portion, B_i, of said buffer to each of said output ports, i, using a sharing approach where each port uses B in their computation of effective bandwidths, as required by claims 4 and 20.

Claim 10

Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Worster, and further in view of Mitra. Regarding claim 10, the Examiner asserts that Mitra discloses allocating the effective buffer space requirement in said node for said admitted circuit (FIG. 4; col. 9, lines 25-67; col. 10, lines 1-23).

Claim 10 requires wherein a set of n admitted virtual circuits, having respective buffer space requirements b_n are already routed through said node and wherein the step of admitting comprises the step of:

routing an $n+1^{th}$ requested virtual circuit through said node with respective associated buffer space requirement b_{n+1} if

$$\sum_{j=1}^{n+1} b_j \leq B$$

.

Appellants, however, could find no disclosure or suggestion by Worster or Mitra that the step of admitting comprises the step of routing an $n+1^{th}$ requested virtual circuit through a node with respective associated buffer space requirement b_{n+1} if

$$\sum_{j=1}^{n+1} b_j \leq B$$

.

Thus, Worster, Mitra, and Elwalid et al. (alone or in combination) do not disclose or suggest wherein a set of n admitted virtual circuits, having respective buffer space requirements b_n are already routed through said node and wherein the step of admitting comprises the step of:

routing an $n+1^{th}$ requested virtual circuit through said node with respective associated buffer space requirement b_{n+1} if

$$\sum_{j=1}^{n+1} b_j \leq B$$

,

as required by claim 10.

Conclusion

The rejections of the cited claims under section §103 in view of Worster and Mitra, alone or in any combination, are therefore believed to be improper and should be withdrawn. The Examiner has already indicated that claims 5 and 21 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

Date: November 28, 2005

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APPENDIX

1. A method for processing a request from a first communications device for a virtual circuit through a network, said network having a plurality of nodes and links, each of said nodes having a plurality of output ports sharing a buffer having a buffer size, B, and each of said links being characterized by a bandwidth capacity, C, said method comprising the steps of:

provisioning a portion, B_i, of said buffer to each of said output ports, i, for use in a computation of effective bandwidth;

receiving a signal representing a request for admission of a virtual circuit in said network for conveying data from said first communications device to a second communication device, the requested virtual circuit to be routed through an access regulator and at least one node connected to a corresponding link of said network, wherein data transmission characteristics of said access regulator are represented by a set of parameters;

determining said effective bandwidth and buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C; and

admitting said virtual circuit request if said determined bandwidth and buffer space requirements are less than available buffer memory space in said buffer and available link bandwidth capacity in said link.

2. The method of claim 1, wherein said set of parameters representing said transmission characteristics of said access regulator comprise a long term average rate, r, a maximum burst size, B_T, and a peak rate, P, and wherein a lossless effective bandwidth requirement e_0 satisfies the expression:

$$e_0 = \frac{P}{1 + \frac{B_i}{C}\frac{(P-r)}{B_T}}$$

3. The method of claim 1, wherein a lossy effective bandwidth, e_l, is obtained from the expression C/K_{max}, where K_{max} is the maximum value of K that satisfies the inequality:

$$P_r\left[\sum_i^K U_i(t) \geq C\right] \leq CLR.$$

4. The method of claim 1, wherein said portion, B_i, of said buffer is allocated to each of said output ports, i, by selecting a value from a range bounded by a lower limit that divides the buffer space, B, among all the ports such that $\sum_i B_i = B_{SMF}$ and an upper limit that allocates said portion, B_i, of said buffer to each of said output ports, i, using a sharing approach where each port uses B in their computation of effective bandwidths.

5. The method of claim 1, wherein a new connection request demanding a buffer size of $b_{l_{new}}$ is admitted if:

$$\sum_j^{J_i} \sum_k^{K_{i,j}} b_{l_{i,j,k}} + b_{l_{new}} \leq \min\left\{ C_i\left(B - \sum_i^N \sum_j^{J_i} \sum_k^{K_{i,j}} b_{l_{i,j,k}} - b_{l_{new}} \right), B_i \right\}$$

6. The method of claim 1, wherein said access regulator is a leaky bucket regulator.

7. The method of claim 1, further comprising the step of allocating said effective bandwidth requirement in said link for said admitted virtual circuit.

8. The method of claim 7, wherein a set of n admitted virtual circuits, having respective bandwidth requirements e_n are already routed through said node and wherein the step of admitting comprises the step of:

routing an $n+1^{th}$ requested virtual circuit through said node with respective associated bandwidth requirement e_{n+1} if:

$$\sum_{j=1}^{n+1} e_j \leq C$$

9. The method of claim 1, further comprising the step of allocating said effective buffer space requirement in said node for said admitted virtual circuit.

10. The method of claim 9 wherein a set of n admitted virtual circuits, having respective buffer space requirements b_n are already routed through said node and wherein the step of admitting comprises the step of:

routing an $n+1^{th}$ requested virtual circuit through said node with respective associated buffer space requirement b_{n+1} if

$$\sum_{j=1}^{n+1} b_j \leq B .$$

11. A method for processing a request from a first communications device for a virtual circuit through a network, said network having a plurality of nodes and links, each of said nodes having a plurality of output ports sharing a buffer having a buffer size, B, and each of said links being characterized by a bandwidth capacity, C, said method comprising the steps of:

provisioning a portion, B_i, of said buffer to each of said output ports, i, for use in a computation of effective bandwidth;

receiving a signal representing a request for a virtual circuit for conveying data from a communication device, the requested virtual circuit to be routed through a node connected to a link, wherein said data arrives at said node at a rate characterized by a set of parameters, said set of parameters including a long term average rate, r, a maximum burst size, B_T, and a peak rate, P;

determining said effective bandwidth and buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C,

obtaining a lossless effective bandwidth requirement, e_0, using the expression:

$$e_0 = \frac{P}{1 + \frac{B_i}{C}\frac{(P-r)}{B_T}}; \text{ and}$$

admitting said virtual circuit request if said determined bandwidth and buffer space requirements are less than available buffer memory space in said buffer and available link bandwidth capacity in said link.

12. The method of claim 11, wherein a set of n admitted virtual circuits, having respective bandwidth requirements e_n are already routed through said node and wherein the step of admitting comprises the step of:

routing an $n+1^{th}$ requested virtual circuit through said node with respective bandwidth requirements e_{n+1} if

$$\sum_{j=1}^{n+1} e_j \leq C .$$

13. The method of claim 11, wherein said set of parameters characterize a function for controlling said rate of data from said communication device.

14. The method of claim 13, wherein said function is performed by an access regulator.

15. The method of claim 14, wherein said access regulator is a leaky bucket regulator.

16. The method of claim 11, further comprising the step of allocating said effective bandwidth requirement in said link for said admitted virtual circuit.

17. The method of claim 11, further comprising the step of allocating said effective buffer space requirement in said buffer for said admitted virtual circuit.

18. The method of claim 11, wherein a set of n admitted virtual circuits, having respective buffer requirements b_n are already routed through said node and wherein the step of admitting comprises the step of:

routing an $n+1^{th}$ requested virtual circuit through said node with respective buffer size requirement b_{n+1} if:

$$\sum_{j=1}^{n+1} b_j \leq B .$$

19. The method of claim 11, wherein a lossy effective bandwidth, e_l, is obtained from the expression C/K_{max}, where K_{max} is the maximum value of K that satisfies the inequality:

$$P_r\left[\sum_i^K U_i(t) \geq C\right] \leq CLR.$$

20. The method of claim 11, wherein said portion, B_i, of said buffer is allocated to each of said output ports, i, by selecting a value from a range bounded by a lower limit that divides the buffer space, B, among all the ports such that $\sum_i B_i = B_{SMF}$ and an upper limit that allocates said portion, B_i, of said buffer to each of said output ports, i, using a sharing approach where each port uses B in their computation of effective bandwidths.

21. The method of claim 11, wherein a new connection request demanding a buffer size of $b_{l_{new}}$ is admitted if:

$$\sum_j^{J_i} \sum_k^{K_{i,j}} b_{l_{i,j,k}} + b_{l_{new}} \leq \min\left\{ C_i\left(B - \sum_i^N \sum_j^{J_i} \sum_k^{K_{i,j}} b_{l_{i,j,k}} - b_{l_{new}} \right), B_i \right\}$$

22. A network node, comprising:

at least one input port for receiving a request from a first communications device for a virtual circuit through a network, said network having a plurality of links, each of said links being characterized by a bandwidth capacity, C;

a plurality of output ports sharing a buffer having a buffer size, B;

a memory for storing computer-readable code; and

a processor operatively coupled to said memory, said processor configured to execute said computer-readable code, said computer-readable code configuring said processor to:

provision a portion, B_i, of said buffer to each of said output ports, i, for use in a computation of effective bandwidth;

receive a signal representing a request for admission of a virtual circuit in said network for conveying data from said first communications device to a second communication device, the requested virtual circuit to be routed through an access regulator and at least one node connected to a corresponding link of said network, wherein data transmission characteristics of said access regulator are represented by a set of parameters;

determine said effective bandwidth and buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C; and

admit said virtual circuit request if said determined bandwidth and buffer space requirements are less than available buffer memory space in said buffer and available link bandwidth capacity in said link.

23. A network node, comprising:

at least one input port for receiving a request from a first communications device for a virtual circuit through a network, said network having a plurality of links, each of said links being characterized by a bandwidth capacity, C;

a plurality of output ports sharing a buffer having a buffer size, B;

a memory for storing computer-readable code; and

a processor operatively coupled to said memory, said processor configured to execute said computer-readable code, said computer-readable code configuring said processor to:

provision a portion, B_i, of said buffer to each of said output ports, i, for use in a computation of effective bandwidth;

receive a signal representing a request for a virtual circuit for conveying data from a communication device, the requested virtual circuit to be routed through a node connected to a

link, wherein said data arrives at said node at a rate characterized by a set of parameters, said set of parameters including a long term average rate, r, a maximum burst size, B_T, and a peak rate, P;

determine said effective bandwidth and buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_0 to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link bandwidth capacity C,

obtain a lossless effective bandwidth requirement, e_0, using the expression:

$$e_0 = \frac{P}{1 + \frac{B_i}{C}\frac{(P-r)}{B_T}}; \text{ and}$$

admit said virtual circuit request if said determined bandwidth and buffer space requirements are less than available buffer memory space in said buffer and available link bandwidth capacity in said link.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.